REMARKS

Prior to entry of the present amendment, claims 54-56, 65-71, 73-80 and 87-114 were pending in the present application. Claims 66, 91, 106 and 110 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The Applicant notes, with appreciation, that the Office Action indicates at page 10, section 36, that claims 54-56 and 65 are allowed.

Claims 66-67, 73-79, 91, 93-96, 101-104, 106, 107, 109, 110 and 112-114 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* (U.S. Patent Number 6,510,503). Claims 68, 97 and 108 stand rejected under 35 U.S.C.103(a) as being unpatentable over Gillingham, *et al.*, in view of Wada, *et al.* (U.S. Patent Number 5,379,248). Claims 69-71, 87-89 and 98-100 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Yoshitake (U.S. Patent Number 6,043,704). Claims 80, 92 and 111 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Moyal, *et al.* (U.S. Patent Number 6,326,853). Claims 90 and 105 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth (U.S. Patent Number 6,029,250). Reconsideration of the rejection and allowance of the claims are respectfully requested.

In the present invention as claimed in claim 66, a memory system having a stub configuration includes a first memory module including a plurality of memory devices, each directly connected to a data bus and a first clock signal line for receiving data signals and a first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal.

In the present invention as claimed in claim 91, a memory system having a stub configuration includes a first memory module including a plurality of memory devices,

each directly connected to a data bus and a first clock signal line for receiving data signals and a first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal.

In the present invention as claimed in claim 106, a method of transferring data in a memory system having a stub configuration includes receiving data signals and a first clock signal at a first memory module including a plurality of memory devices, each directly connected to a data bus and a first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal at a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively.

In the present invention as claimed in claim 110, a method of transferring data in a memory system having a stub configuration includes receiving data signals and a first clock signal at a first memory module including a plurality of memory devices, each directly connected to a data bus and a first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal, at single a control/address buffer device.

Gillingham, *et al.*, in FIG. 8(a) discloses a memory device interface circuit that is an input circuit included in a memory device. A command and data interface section 98 of the memory device interface provides even clock CLK_E and odd clock CLK_O signals which latch even and odd row commands row_E, row_O as well as even and odd column commands col_E, col_O into the core DRAM via D-type flip-flops 106 (Gillingham, *et al.*, column 10, line 58 – column 11, line 22). Separate programmable

fine vernier delays 107 and 108 receive as inputs the clock signal CLK and delay the rising and falling edges of the clock signal CLK to generate delayed signals OUTCLKE and OUTCLKO (Gillingham, *et al.*, column 11, lines 22-26). These OUTCLKE and OUTCLKO signals drive the clock input of respective D-type latches 120 and 122 for latching the even Data_Out_E and odd Data_Out_O output data signals from the core DRAM (Gillingham, *et al.*, column 11, lines 26-28). The data read from the memory, or input to the memory, is synchronized with data clocks dclk0 and dclk1. In this manner, the Gillingham, *et al.* embodiments illustrate that each memory device interface circuit (for example of the type depicted in FIG. 8a) is responsible for transferring signals, including row and column command signals, to and from a <u>single</u>, corresponding, memory device (for example, memory device 84 of FIG. 7, memory device 100 of FIG. 8a, and memory device 174 of FIG. 13a) in the memory system. Therefore, each memory device 84, 100, 174 in Gillingham, *et al.* includes such a memory device interface circuit and, thus, each memory device includes the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108 of the memory device interface circuit. In FIG. 12 of Gillingham, *et al.*, a buffered module 160 includes two memory devices 162 and a buffer 164. The buffer 164 supplies the row and column command streams and clock signal CLK to each of the memory devices 162 on the buffered module 160, while read data and write data are clocked by their respective data clocks dclkA and dclkB. Each memory device 162 on the buffered module 160 is connected to the clock signal CLK through the buffer 164. Each of the memory devices 162 includes the memory device interface circuit including the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108.

With regard to claim 66, Gillingham, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and

the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed. In Gillingham, *et al.*, each memory device 84, 100, 174 includes the memory device interface circuit and, thus, each memory device includes the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, and associated circuitry, that collectively are asserted in the Office Action at page 2, paragraph 3, line 9 as being analogous to the "control/address buffer device" of claim 66. Therefore, in Gillingham, *et al.*, a single memory device interface circuit, including the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, supplied the column commands and row commands to a single, corresponding, memory device, and, therefore, Gillingham, *et al.* fails to teach or suggest a "single control/address buffer device" included on the "first memory module" that supplies the "control signal and the address signal to each of the plurality of memory devices", as claimed in claim 66. Rather, in Gillingham, *et al.*, a single memory device interface circuit supplies the column commands and row commands to a single, corresponding, memory device. While FIG. 12 of Gillingham, *et al.* illustrates an embodiment where the buffer 164 supplies the row and column command streams and clock signal CLK to the memory devices 162, each memory device 162 in this embodiment receives the clock signal CLK through the buffer 164 and does not receive the clock signal directly from the controller 165. Therefore, the memory devices 162 are not each directly connected to the clock signal CLK. Thus, Gillingham, *et al.* fails to teach or suggest "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively", as claimed in claim 66.

With regard to the claim 91, Gillingham, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the

address signal to each of the plurality of memory devices in response to the first clock signal", as claimed. In Gillingham, *et al.*, each memory device 84, 100, 174 includes the memory device interface circuit and, thus, each memory device includes the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, and associated circuitry, that collectively are asserted in the Office Action at page 2, paragraph 3, line 9. as being analogous to the "control/address buffer device" of claim 91. Therefore, in Gillingham, *et al.*, a single memory device interface circuit, including the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, supplied the column commands and row commands to a single, corresponding, memory device, and, therefore, Gillingham, *et al.* fails to teach or suggest a "single control/address buffer device" included on the "first memory module" that supplies the "control signal and the address signal to each of the plurality of memory devices", as claimed in claim 91. Rather, in Gillingham, *et al.*, a single memory device interface circuit supplies the column commands and row commands to a single, corresponding, memory device. While FIG. 12 of Gillingham, *et al.* illustrates an embodiment where the buffer 164 supplies the row and column command streams and clock signal CLK to the memory devices 162, each memory device 162 in this embodiment receives the clock signal CLK through the buffer 164 and does not receive the clock signal directly from the controller 165. Therefore, the memory devices 162 are not each directly connected to the clock signal CLK. Thus, Gillingham, *et al.* fails to teach or suggest "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively", as claimed in claim 91.

With regard to claim 106, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal at a single control/address buffer device that

is connected to the control signal line, the address signal line and the first clock signal line respectively", as claimed. In Gillingham, *et al.*, each memory device 84, 100, 174 includes the memory device interface circuit and, thus, each memory device includes the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, and associated circuitry, that collectively are asserted in the Office Action at page 2, paragraph 3, line 9 as being analogous to the "control/address buffer device" of claim 106. Therefore, in Gillingham, *et al.*, a single memory device interface circuit, including the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, supplied the column commands and row commands to a single, corresponding, memory device, and, therefore, Gillingham, *et al.* fails to teach or suggest a "single control/address buffer device" included on the "first memory module" that supplies the "control signal and the address signal to each of the plurality of memory devices", as claimed in claim 106. Rather, in Gillingham, *et al.*, a single memory device interface circuit supplies the column commands and row commands to a single, corresponding, memory device. While FIG. 12 of Gillingham, *et al.* illustrates an embodiment where the buffer 164 supplies the row and column command streams and clock signal CLK to the memory devices 162, each memory device 162 in this embodiment receives the clock signal CLK through the buffer 164 and does not receive the clock signal directly from the controller 165. Therefore, the memory devices 162 are not each directly connected to the clock signal CLK. Thus, Gillingham, *et al.* fails to teach or suggest "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal", as claimed in claim 106.

With regard to claim 110, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the

plurality of memory devices in response to the first clock signal, at a single control/address buffer device", as claimed. In Gillingham, *et al.*, each memory device 84, 100, 174 includes the memory device interface circuit and, thus, each memory device includes the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, and associated circuitry, that collectively are asserted in the Office Action at page 2, paragraph 3, line 9 as being analogous to the "control/address buffer device" of claim 110. Therefore, in Gillingham, *et al.*, a single memory device interface circuit, including the D-type flip-flops 106 and the programmable fine vernier delays 107 and 108, supplied the column commands and row commands to a single, corresponding, memory device, and, therefore, Gillingham, *et al.* fails to teach or suggest a "single control/address buffer device" included on the "first memory module" that supplies the "control signal and the address signal to each of the plurality of memory devices", as claimed in claim 110. Rather, in Gillingham, *et al.*, a single memory device interface circuit supplies the column commands and row commands to a single, corresponding, memory device. While FIG. 12 of Gillingham, *et al.* illustrates an embodiment where the buffer 164 supplies the row and column command streams and clock signal CLK to the memory devices 162, each memory device 162 in this embodiment receives the clock signal CLK through the buffer 164 and does not receive the clock signal directly from the controller 165. Therefore, the memory devices 162 are not each directly connected to the clock signal CLK. Thus, Gillingham, *et al.* fails to teach or suggest "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal", as claimed in claim 110.

Accordingly, reconsideration and removal of the rejection of independent claims 66, 91, 106 and 110 under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* are therefore respectfully requested. With regard to dependent claims 67, 73-79, 93-96, 101-104, 107, 109 and 112-114, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejections of claims 68, 97 and 108, Wada, *et al.* is cited in the Office Action as disclosing a memory system wherein first and second signal lines are crossed on the motherboard between the first and second modules.

Like Gillingham, *et al.*, Wada, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 68. Like Gillingham, *et al.*, Wada, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 97. In addition, like Gillingham, *et al.*, Wada, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal at a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively", as claimed in claim 108.

Neither Gillingham, *et al.* nor Wada, *et al.* teaches or suggests the present invention as claimed in claims 68, 97 and 108. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Wada, *et al.* fails to teach or suggest the invention as claimed in claims 68, 97 and 108. Reconsideration of the rejection of, and allowance of claims 68, 97 and 108 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Wada, *et al.* are respectfully requested.

With regard to the rejection of claims 69-71, 87-89, 98-100, like Gillingham, *et al.*, Yoshitake fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claims 69-71 and 87-89. Like Gillingham, *et al.*, Yoshitake further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claims 98-100.

Neither Gillingham, *et al.* nor Yoshitake teaches or suggests the present invention as claimed in claims 69-71, 87-89 and 98-100. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Yoshitake fails to teach or suggest the invention as claimed in claims 69-71, 87-89 and 98-100. Reconsideration of the rejection of and

allowance of claims 69-71, 87-89 and 98-100 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Yoshitake are respectfully requested.

With regard to the rejections of claims 80, 92 and 111, like Gillingham, *et al.*, Moyal, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 80. Like Gillingham, *et al.*, Moyal, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 92. In addition, like Gillingham, *et al.*, Moyal, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal, at a single control/address buffer device", as claimed in claim 111.

Neither Gillingham, *et al.* nor Moyal, *et al.* teaches or suggests the present invention as claimed in claims 80, 92 and 111. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Moyal, *et al.* fails to teach or suggest the invention as claimed in claims 80, 92 and 111. Reconsideration of the rejection of, and allowance of claims 80, 92 and 111 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Moyal, *et al.* are respectfully requested.

With regard to the rejection of claims 90 and 105, like Gillingham, *et al.*, Keeth fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each directly connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a single control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 90. Like Gillingham, *et al.*, Keeth further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including a plurality of memory devices, each connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a single control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to each of the plurality of memory devices in response to the first clock signal", as claimed in claim 105.

Neither Gillingham, *et al.* nor Keeth teaches or suggests the present invention as claimed in claims 90 and 105. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Keeth fails to teach or suggest the invention as claimed in claims 90 and 105. Reconsideration of the rejection of, and allowance of claims 90 and 105 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Keeth are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Authorization is hereby given to charge Deposit Account No. 50-1798 for all fees due with this response.

Respectfully submitted,

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